FPGA Architecture in Finance

Future state market data and trading architecture

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FPGA Architecture

- FPGA Generic Use Cases
  - FIX to binary translation
    - Common format conversion
      - C structure, Protocol Buffers, MessagePack, LBM
  - Multicast Emission
    - BGP/IGMP session management and address readvertisement
  - Rules Engine
    - Risk checks
  - Crossing Engine
    - Highly scalable and performant
  - Book building
  - Kill switch
  - Flow capture (drop copy/exchange flow)
  - High-accuracy packet timestamping
  - Virtualisation: data deduplication

FPGA On A Network Switch

- **Market Connectivity/Session Management**
  - Timed log on/off
  - Kill switch
  - Throttle Management
    - Buffer or reject
  - Feed arbitration
  - Network/Exchange jitter collection/analytics
  - IGMP/BGP/AS/Address readvertising
  - IP filtering
    - Security

- **Market Data**
  - Multicast rebroadcast by group/port or topic (LBM)
  - Port forwarding to many downstream systems
  - Feed shredding
  - Protocol conversion
    - Protocol Buffers/MessagePack/LBM
  - Symbol Conversion and substitution
    - Dictionary, ontology
    - Order id lookup

FPGA On A Network Switch

- **Trading**
  - Trade emission from template
    - Reduced PCIe and network traffice
  - Risk Checks
- Generic/per-client risk checks
- Feed/ Stats rebroadcast

- **Distributed order management**

FPGA On A Network Interface Card - Ingress

- **Receiver Side Steering**
  - Symbol shredding
  - Work queue allocation based on queue stats
- **Kernel bypass bypass**
  - NIC buffer access in user address space
  - VMA from Mellanox and ef_vi from Solarflare
- **Accelerated 29West**
  - Mellanox have this already
  - Solarflare are collaborating with 29West on this currently
- **DDI (SandyBridge)**
  - direct injection to level three cache
- **Rules based Packet/Trade Filtering**
  - Application never sees irrelevant trades

FPGA On A Network Interface Card - Egress

- **Trade templates**
  - Parameterised orders
  - Minimising transmission pacing (contention on PCIe bus)
- **Strategy controlled QOS**
  - priority marking of trades
- **Risk Checks**
  - Per-client trading/risk/order management checks
- **Inter NIC communication**
  - via QPI/PCIe 3.0
  - Shared state/reflective memory
    - Distributed Order Management
- **Dynamic Route Selection**
  - Microwave/Fibre route selection based on QOS or latency

SolarFlare FPGA Development Environment

- Altera Developer kit
  - Qaurtus II – free web based version
  - Avalon Verification Suite
  - Free online training
- Solarflare AOE FDK – Firmware Development Kit
  - API, Applications, Libraries, Documentation
  - Applications written in System Verilog
- Generic FPGA Modules
- Applications
  - A/B Arbitration with histogram