Efficient Photonic Coding

Yury Audzevich, Philip Watts,
Sean Kilmurray, Andrew W. Moore

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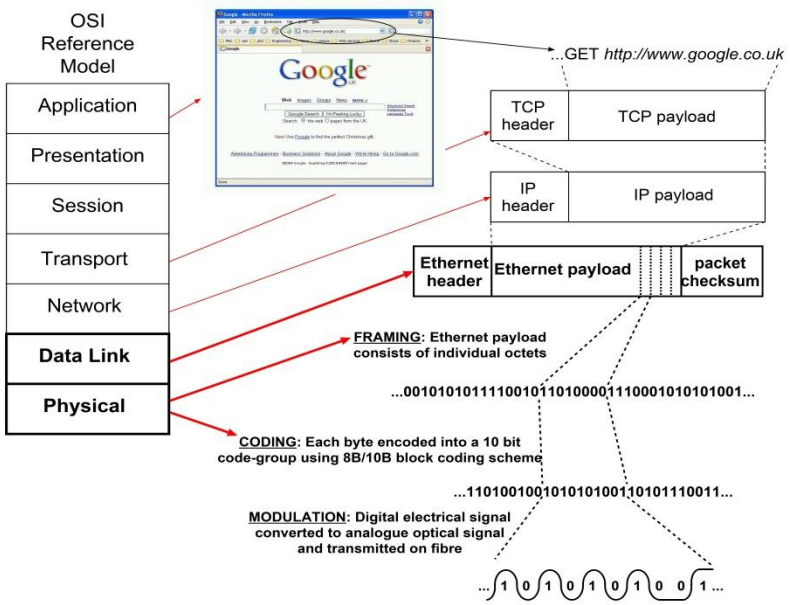
Introduction

Energy-efficiency of transmission systems is one of the key priorities with respect to the next generation of networking equipment. Within this work we aim at providing energy saving solutions for communication networks by:

1) Evaluating energy contributions related to different parts of the communication system focusing on 'lower layer' transmission protocols

2) Quantification of energy effect of DC-balanced codes on the optical transmission system with respect to the optical power requirement and power consumption of coding blocks



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Energy characteristics of DC-balanced codes

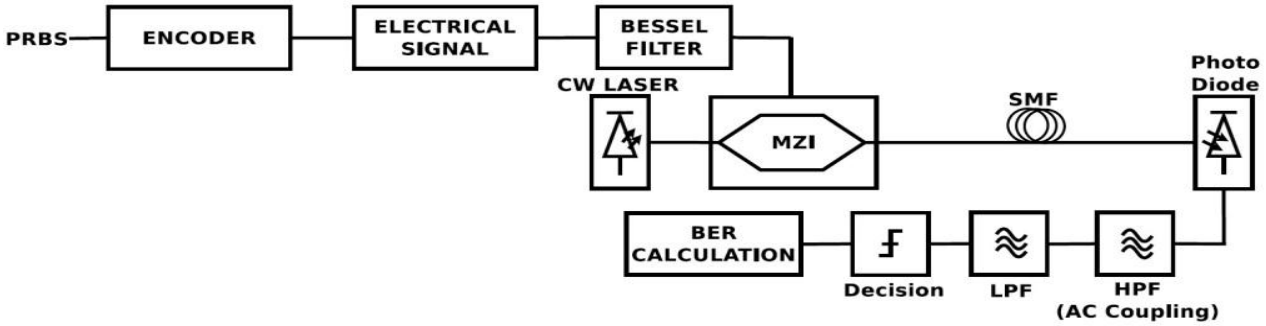
DC-balanced codes provide a reliable transmission over the channel with a benefit of self-synchronization and error detection mechanisms.

Unfortunately, power characteristics of DC-balanced codes are not well investigated.

Three directions are considered:

1) Evaluation of the **optical power requirement** considering 10Gb/s point-to-point links for a variety of coding schemes by means of semi-analytical approach
2) Estimation of the power consumption of **DC-balanced coding** blocks using a CMOS ASIC synthesis flow and its further comparison to the optical power requirement
3) Comparative power analysis of the above codecs is considered for two different technology processes, represented by **90nm UMC90** library and, a low leakage, **45nm Nangate45** library

10Gb/s optical link simulations



Optical link – transmission system:

- A filtered electrical signal waveform from encoder is used to drive MZI
- 2^{19} bits PRBS is used as an input, the baud rate *is adjusted* proportionally to the number of bits from encoder

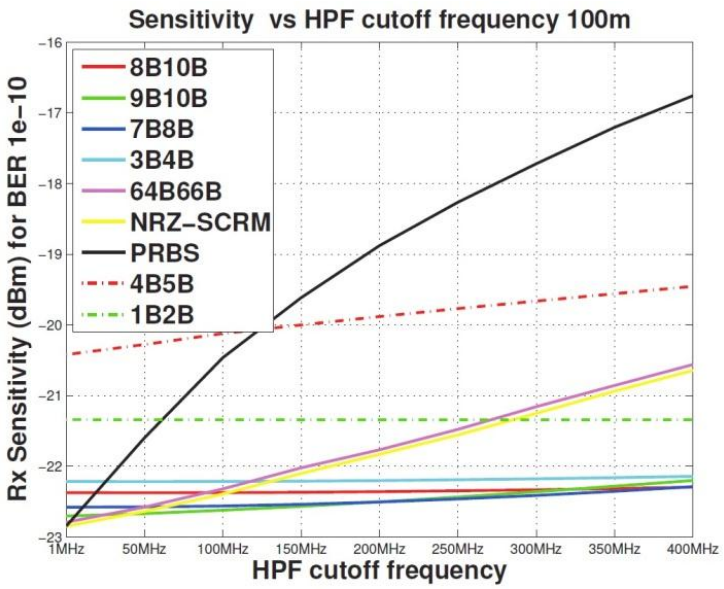
Optical link parameters:

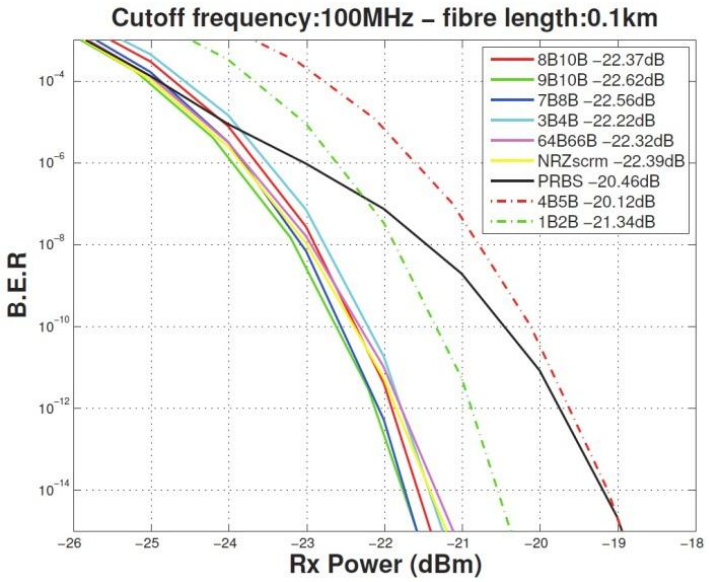
- *100m SMF* with parameters satisfying requirements for 10Gbps Ethernet over SMF

Optical link – receiving system:

- Optical receiver uses a square law direct detector, with *AC coupling* achieved using HPF (with varies cut-off frequencies)
- Sampling point was set at half the bit period and the BER is calculated for a range of received optical power using the complementary error function

10Gb/s optical link simulations (cont.)





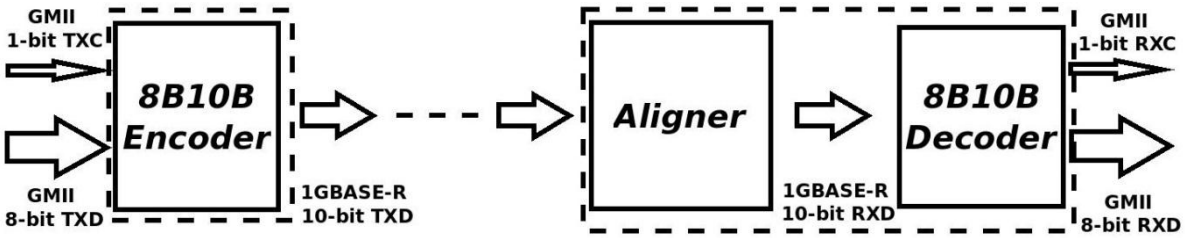
- The mBnB DC-balanced codes are *relatively insensitive* to the cut-off frequency while PRBS data have steady decrease in the receiver sensitivity

- Taking 100MHz HPF cut-off frequency and assuming 20dB link budget, the laser power requirement is *-0.46dBm for uncoded signal* and *-2.2dBm for both 8B10B and 64B66B line codes (0.3mW of savings in optical power)*

Line Coding Blocks – 8B10B and 64B66B

8B10B – parity-disparity DC-balanced code:

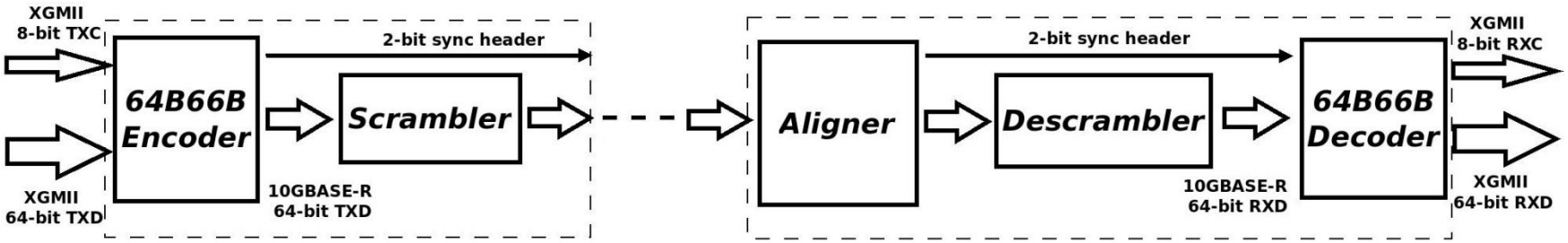
1) Encoder/Decoder – decoding from GMII format into 1GBASE-R format plus *disparity control check* for DC-balance of code words



64B66B coding is implemented using:

1) Encoder/Decoder – decoding from XGMII format into 10GBASE-R format

2) Scrambler/Descrambler – mixing of data to avoid long sequences of 0s/1s



Line Coding – Power Analysis

Implementation:

❖ Behavioural-level 8B10B and 64B66B line coding models (Verilog HDL) are *synthesized* into a gate-level netlist using *technology process libraries* by means of *Synopsis Design Compiler*

❖ Technology process libraries - 90nm UMC90 CMOS library and 45nm Nangate45 CMOS library; these provide *definitions*, *logical descriptions* and *timing information* of logical gates

Verification:

❖ Post-synthesis verification is performed using a test bench with various custom input patterns; *gate-level switching activity* is logged as a Verilog Charge Dump file

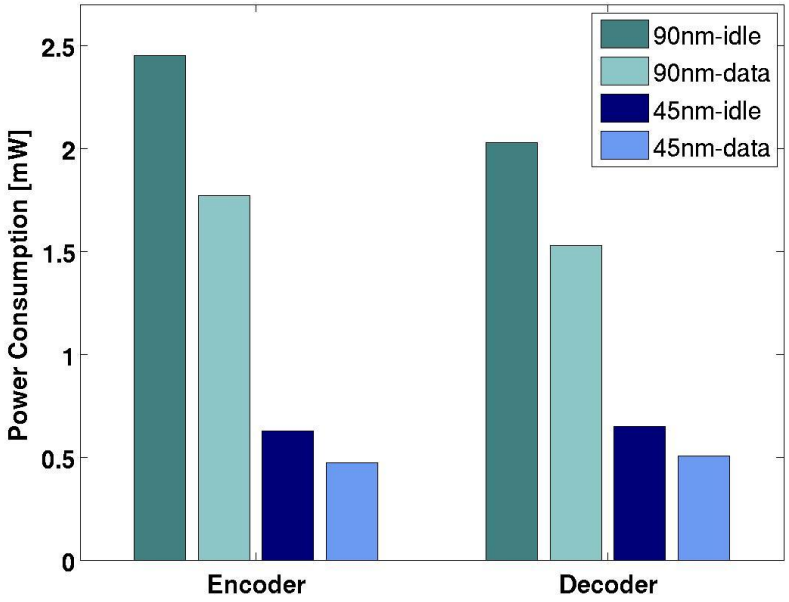
❖ A realistic bit sequence is used as an input for 8B10B/64B66B coding blocks

Power estimations:

❖ Synopsis Prime Time PX suite provides *static and dynamic power group estimates*; based on semantic netlist, VCD file and UMC90 library definitions.

Power estimates – 8B10B

10Gb/s link results: Results obtained *30 microseconds* simulation periods, with a symbol clock frequency of *1.25GHz* for both *45nm and 90nm* tech. process

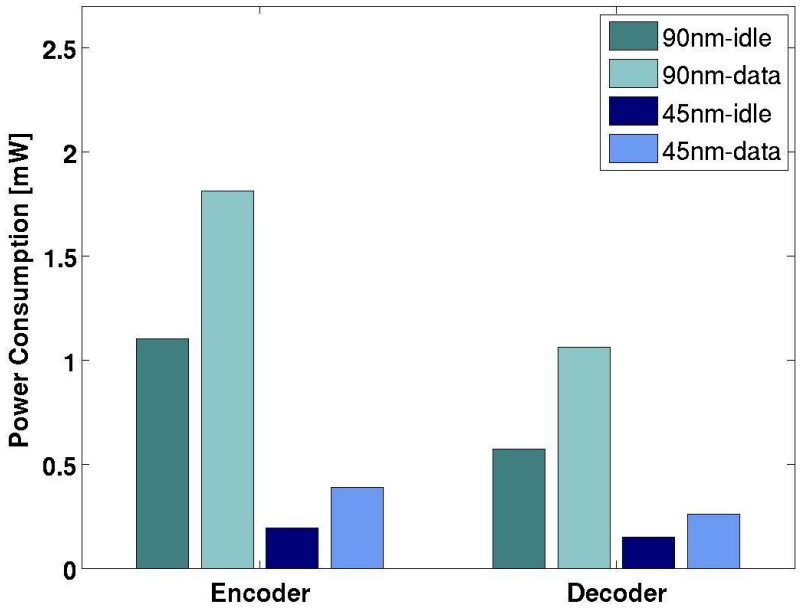


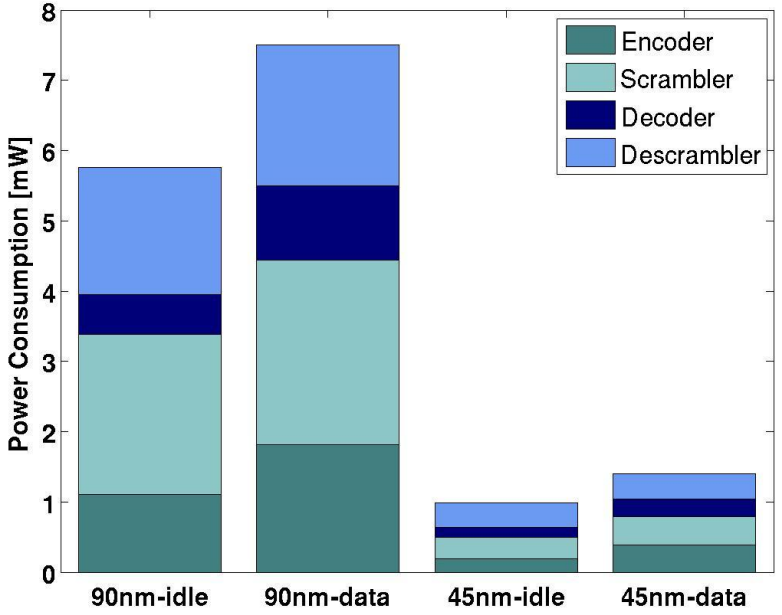
- *IDLE sequences* produce *imbalanced code words,* involving the disparity control check *every clock cycle*
- As a result, the *power consumption* of encoder/decoder in *IDLE state is higher* than in case of a real data traffic!
- Low leakage Nangate45 library provides decrease in power *by the factor of 4*

Power estimates – 64B66B

10Gb/s link results: Identical trace files (to 8B10B simulation) were used for *30 microseconds* simulation periods, with a symbol clock frequency of 156.25 MHz

- **Coding:** *8 X 8-bit* sequences are processed in parallel each clock cycle irrespective on the incoming sequence type (data, control, or mixture of both); During pure data arrivals extra *memory resources* are used for storing and forwarding
- **Scrambling:** 64-bits are scrambled *in parallel* during a clock cycle independently on the arriving sequence's type
- *The combined power cost* of scrambler and descrambler is *1.5-2.5 times larger* than the combined cost of encoder and decoder blocks





Energy-efficient MAC

Observations:

- Current implementations of Ethernet standards require continuous transmission of ***IDLE code words*** (even in the absence of MAC traffic) to avoid ambiguity at the receiver side, e.g. for synchronization, DC-balance, error correction

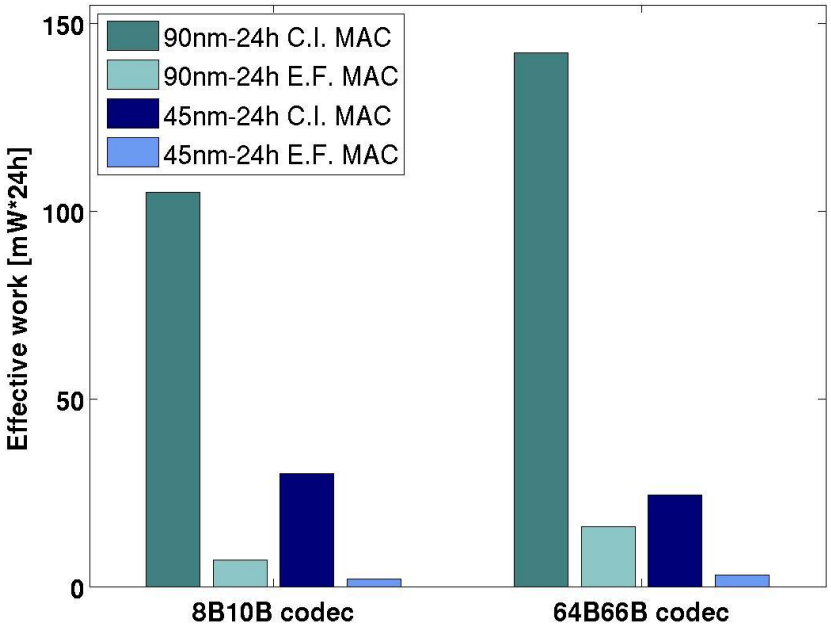
- The majority of the networks are overprovisioned to sustain peak loads and underutilized most of the time

- Our recent analysis of a 24 hours trace file (obtained from a 10Gbps interface) showed average link utilization of **8.79% -** consistent with data-center network utilization

Our approach - reduce unnecessary use of codecs!

Considering the av. Ethernet frame size of **1150bytes** with **64bits** of preamble, the effective savings achieved by switching off (when no real data present) coding blocks can be as high as 93% - depends on the link utilization

Ongoing work and Challenges



Default – off Media Access Control scheme:

- **Power down** of encoding blocks when no real MAC data is present on the link
- Using of a synchronization **preamble** prior to transmission for clock and data recovery (CDR)
- Use of the **burst mode receiver** / **injection locking technique** for the fast and efficient clock and data recovery

Acknowledgements

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Thank you!