Exploring Chip to Chip Photonic Networks

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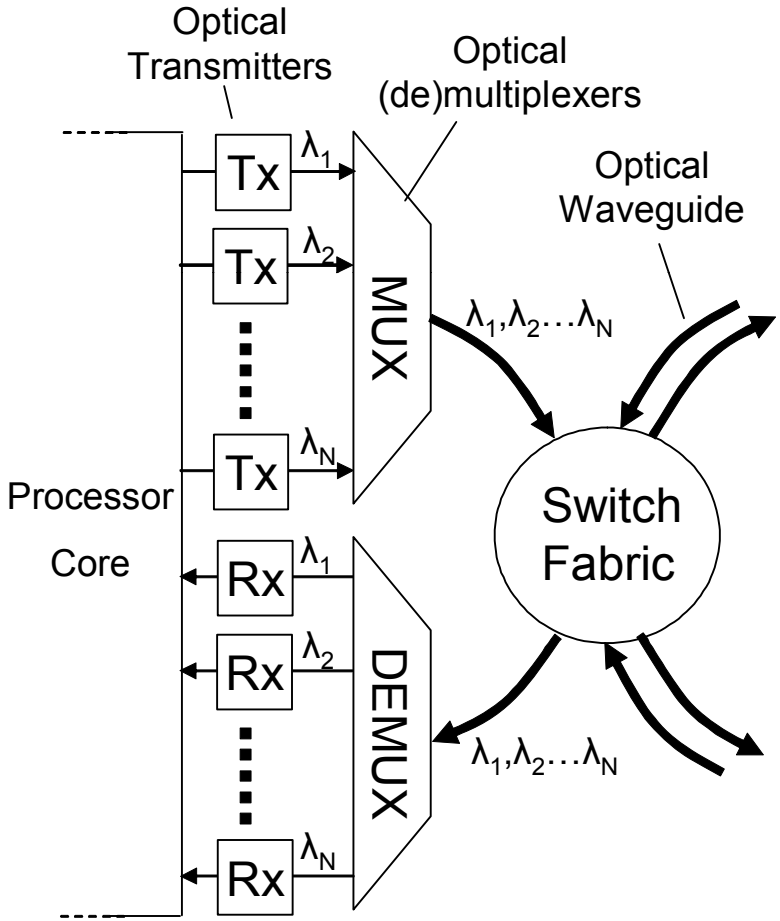
Exploring Chip-to-Chip Photonics

- Bandwidth improvements in electronic interconnects have been achieved at the expense of increased latency and power consumption
- Photonics has the potential to reduce power consumption/ latency
  - Known for a long time, BUT size, cost, manufacturing issues
  - Enabling technologies: silicon photonics and 3D integration
- Needs a holistic, **system** assessment
  - assessing power consumption and performance

Photonics: Low Power and Latency ?

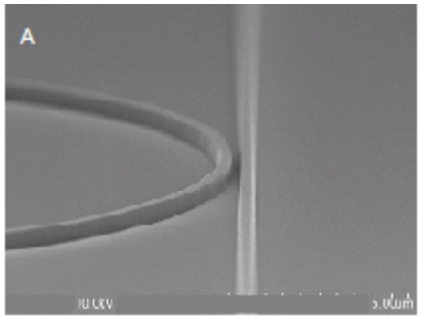
- For point-to-point links:
  - Photonics power consumption is not dependent on distance, only on modulator/detector capacitance
    - Electrical interconnect power increases exponentially with distance
  - Photonics is not pin limited
    - Large bandwidth, low latency using by wavelength multiplexing
- Switched systems:
  - Photonics switching power is not dependent on bandwidth
    - Electronic routers, power and latency consumed for each hop/buffer
- Electronic/Photonic comparisons are highly dependent on assumptions and application



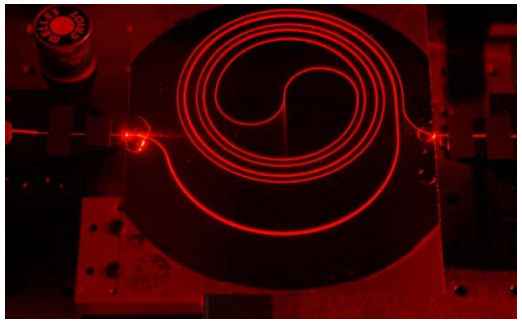
Enabling Technology 1: Silicon Photonics

What's changed?

- Compact waveguides in Si/SiO_2
  - Compact and low cost



Source: Intel



1.4m long spiral polymer waveguide with input from HeNe laser

- Off-chip, polymer waveguides
  - Integration on Copper PCBs

- Ring resonators can modulate, switch and filter
  - Switch/Modulate at >10Gb/s

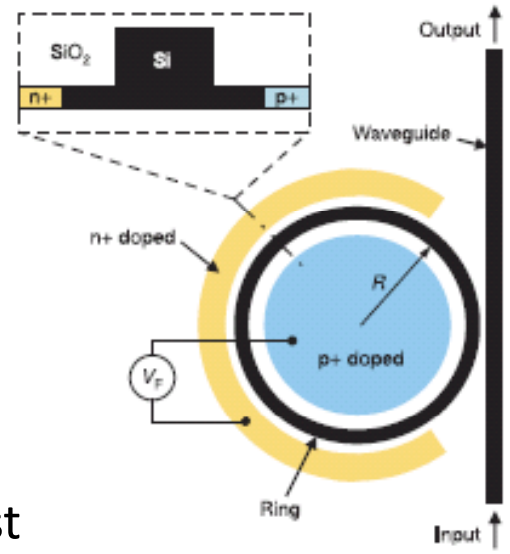
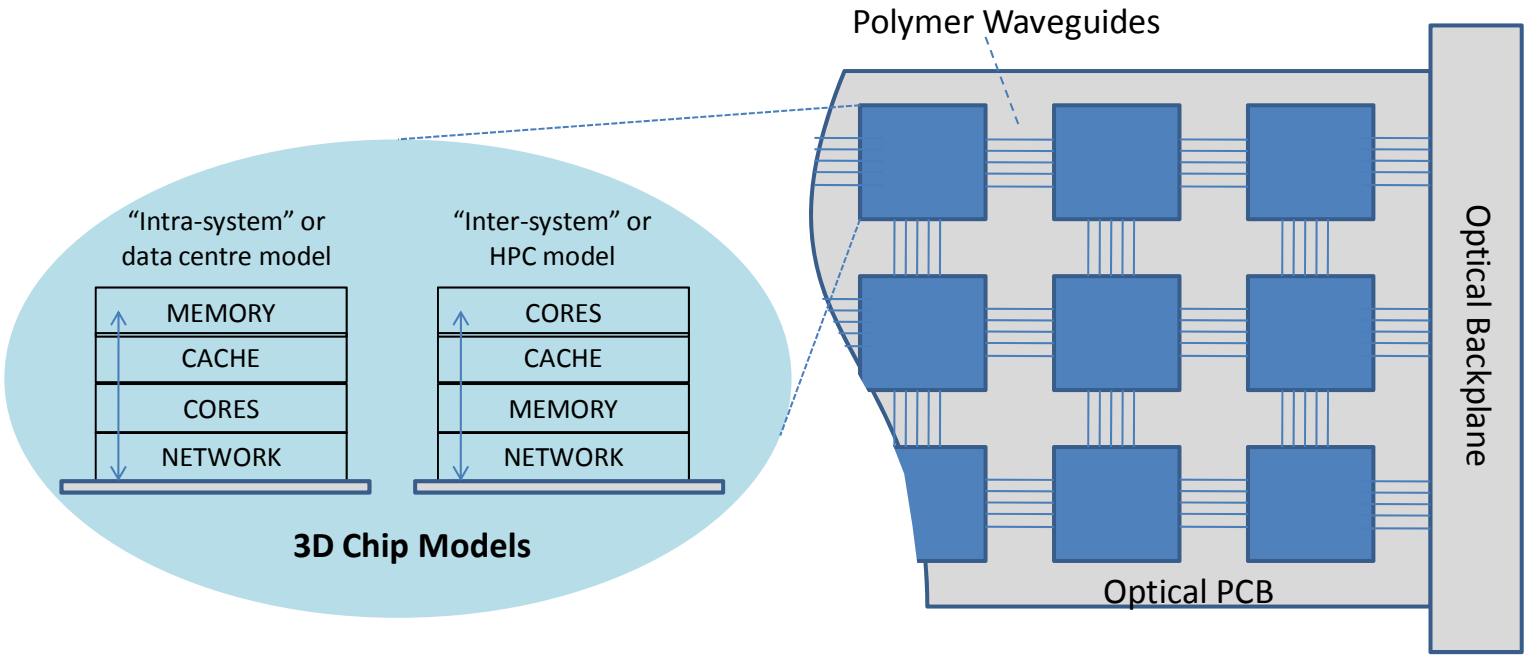


Diagram: M. Lipson (Cornell)

Appropriate detectors and light-sources already exist

Enabling Technology 2: 3D Integration

- Recent advances in 3D point toward multiple cores + DRAM layers (≈1 GB) + network within a single package
- Combine such modules to produce larger systems for data centres or high performance computing
- III-V substrates for light sources can be integrated

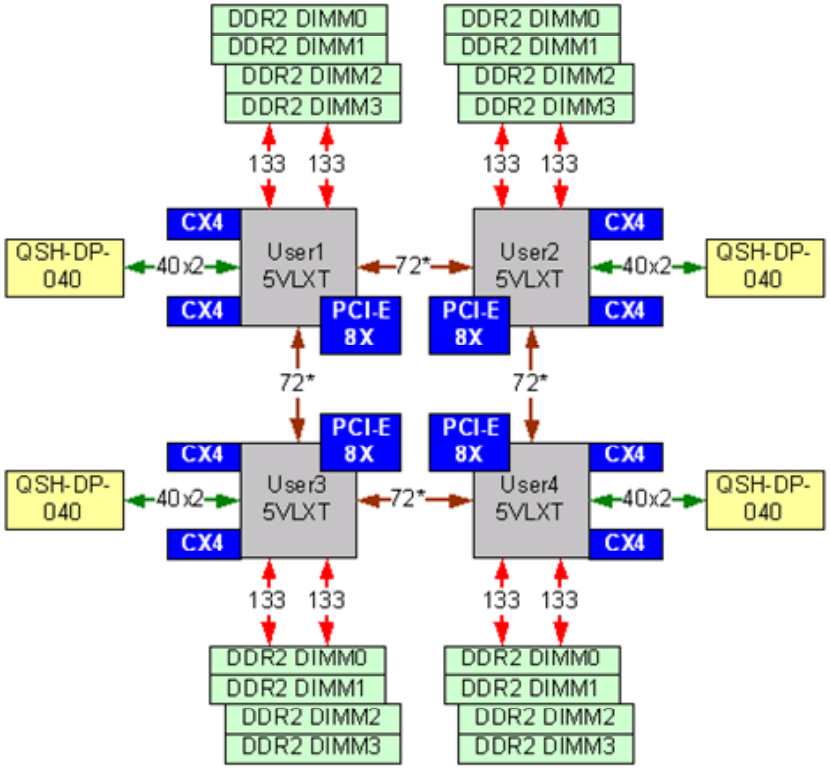


Characteristics of a Photonic Network

- Photonic Limitations:
  - Signals can not be (practically) buffered
  - Difficult to read header and setup switch on the fly
- These limitations leads naturally to circuit switching (with edge buffers)
  - Photonics is good for flows/large packets
  - Relatively inefficient for small packets (e.g. cache lines)
- Obvious network choice: Central Xbar/Clos switch with time slot access, e.g. SWIFT (Intel/Cambridge)
  - Various alternative distributed approaches proposed

FPGA-based Full System Emulation

- FPGA-based emulation enables full system power/performance data using realistic workloads/timescales
  - **100x** faster than software simulation
  - Existing Computer Lab project, C3D, provides BEE3 infrastructure, cores and all-electronic reference design
- Emulate 1000+ core computer with photonic chip-to-chip network model
  - 4 high-end FPGAs per board
  - 4-8 MIPS-64 cores per FPGA
  - Clock rate ≈ 100 MHz
- Levels of model abstraction
  - Parameterisable and synthesisable SystemVerilog network model
  - Photonic component power consumption model
  - Photonic path viability model



Features of BEE3 board (UC Berkeley/Microsoft)

Exploring Chip-to-chip Photonics

- Collaborators: Myself, Andrew Moore, Simon Moore (Cambridge), Robert Killey (UCL EE)
- Program to investigate implications of chip-to-chip photonic interconnect on architecture of:
  - Data Centres
  - High Performance Computing
- Build accurate and experimentally verified models of latest silicon photonics components (UCL)
- Build full system FPGA-based emulator
  - Allows rapid network architectural exploration
  - Find applications which benefit from photonic networks